Memory Characterization, Verification and Simulation

CharFlo-Memory!™
MSIM™
Turbo-MSIM™

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Leader in IP Characterization and Critical-Path Simulation

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Agenda

- Introduction
- Characterization and Simulation for Commercial Memory Compiler Users
- Characterization and Simulation for In-house Memory Compiler Developers
- Circuit Simulation for Characterization and Verification
- Conclusion

Characterization and Simulation

Embedded Memory in SoC Designs

- Majority of SoC chip area could be memory IP
- Multiple sources of memory IP are available
- Legend provides a total solution of characterization and simulation with best price-performance
  - Major commercial/in-house memory compilers
  - All instances of each compiler, which could be several hundred thousand configurations
  - All SPICE models from major foundries
  - Need for push-button and full automation

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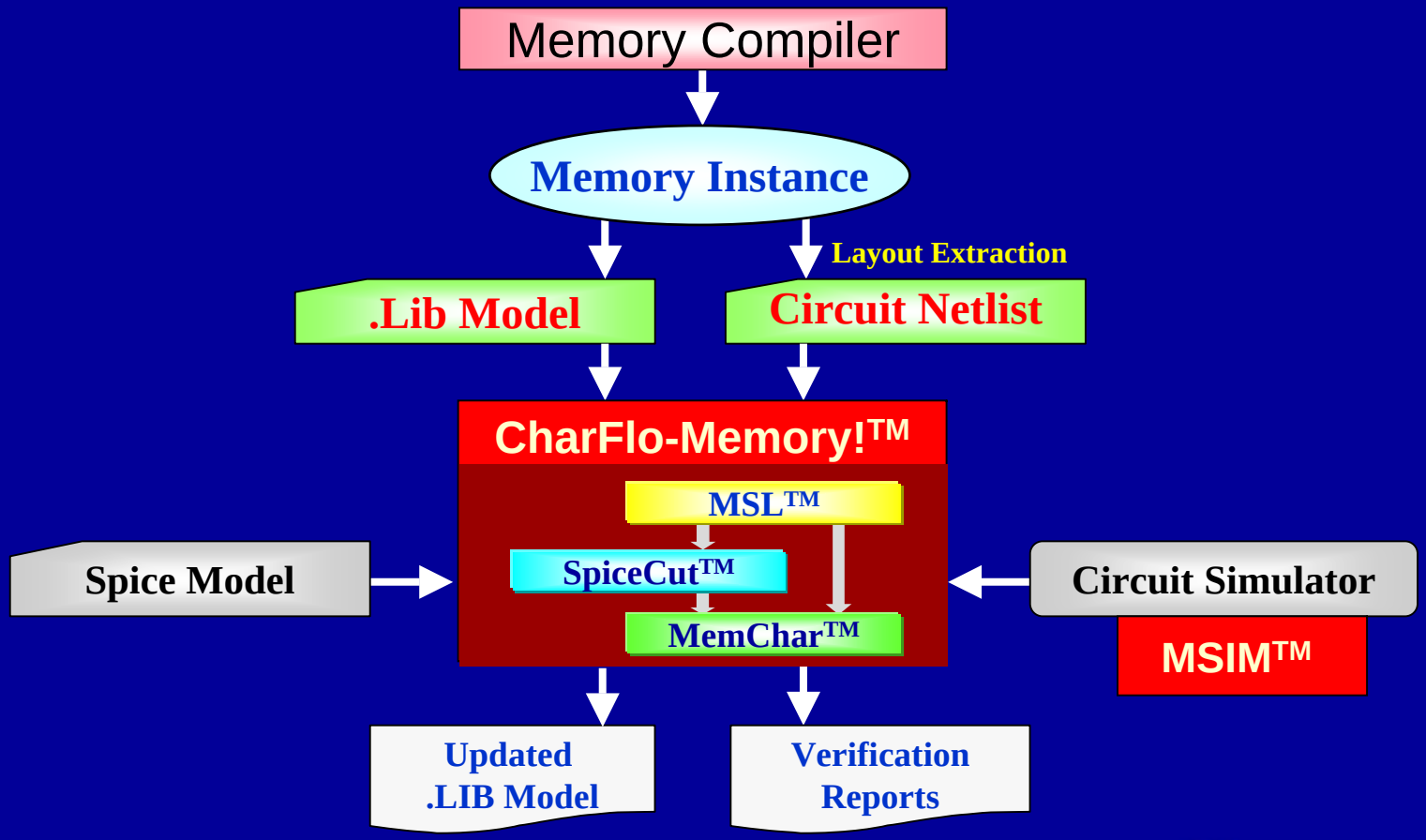
Push-button Characterization Flow



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Push-button Characterization Flow

- **MSL™ :**

  MemChar SpiceCut Library, the tool for automating memory characterization with '.Lib-in and .Lib-out'

- **SpiceCut™ :**

  Critical-path circuit building tool based on layout-extraction with RCs

- **MemChar™ :**

  Memory characterization tool with optimization.

- **MSIM™ :**

  High-accuracy circuit simulator

- **Turbo-MSIM™ :**

  High-speed and high-capacity circuit simulator

Characterization/Simulation for Commercial Compiler Users

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Characterization/Simulation
Users of Memory Compilers

- Perform ***What-if*** analysis
  - Temperature, power supply, PVT's, etc.
- Verify memory IP
  - Re-targeting, e.g. 0.25um to 0.22um
  - Porting to multiple foundry sources
  - Process revision
- Accurate models for low-power/high speed designs

Legend provides a "push-button" solution !

Commercial Compiler Support

Full Automation and Production Proven

Legend provides the 'push-button' automation of instance characterization for following vendors' memory compilers

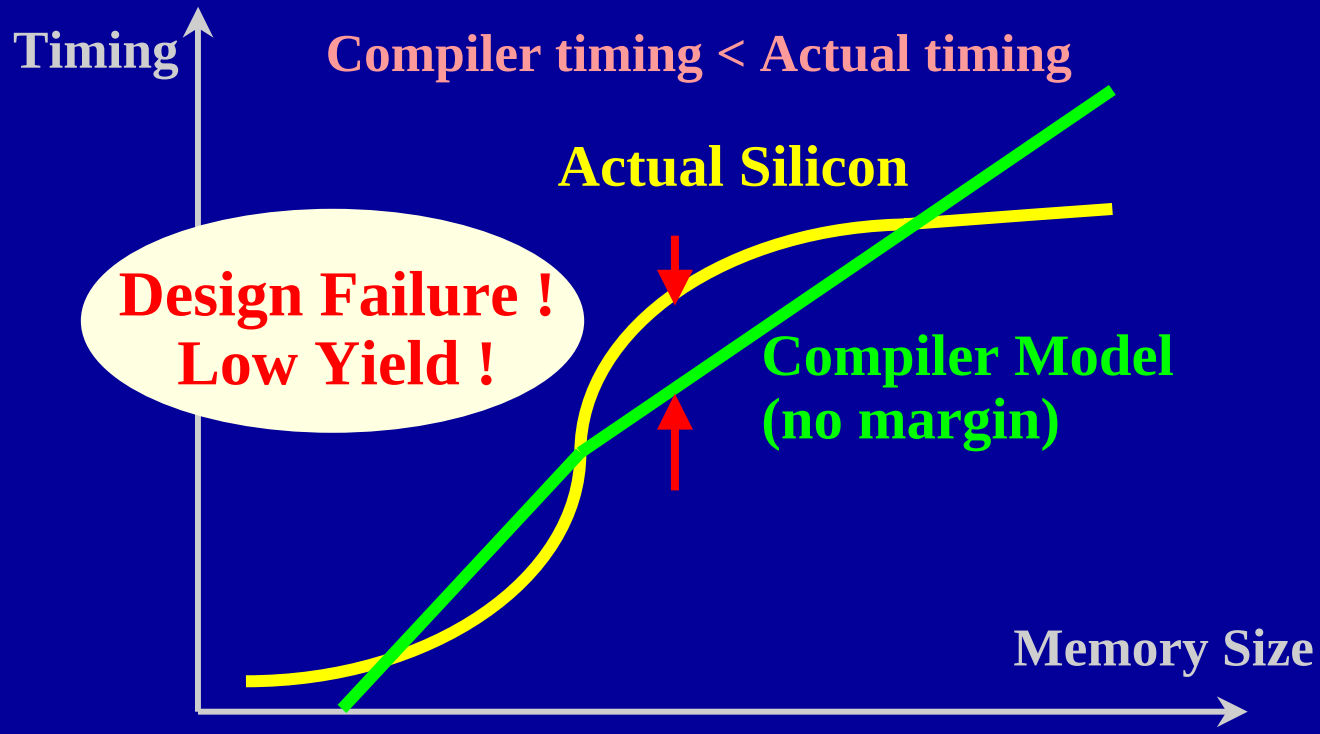
Vendors' Memory Compilers	0.13 um	0.15um	0.18um
Artisan*	**YES**	**YES**	**YES**
Virage	**YES**	**YES**	**YES**
TSMC*	**YES**	*N/A*	*N/A*
Faraday*	**YES**	**YES**	**YES**
Synopsys (Avanti)	*N/A*	*N/A*	**YES**
Dolphin Technology*	**YES**	*Future plan*	*Future plan*
VeriSilicon*	*N/A*	**YES**	**YES**

**** Legend's customer and/or partner***

N/A means indicated compilers not available from vendors

Modeling Inaccuracy

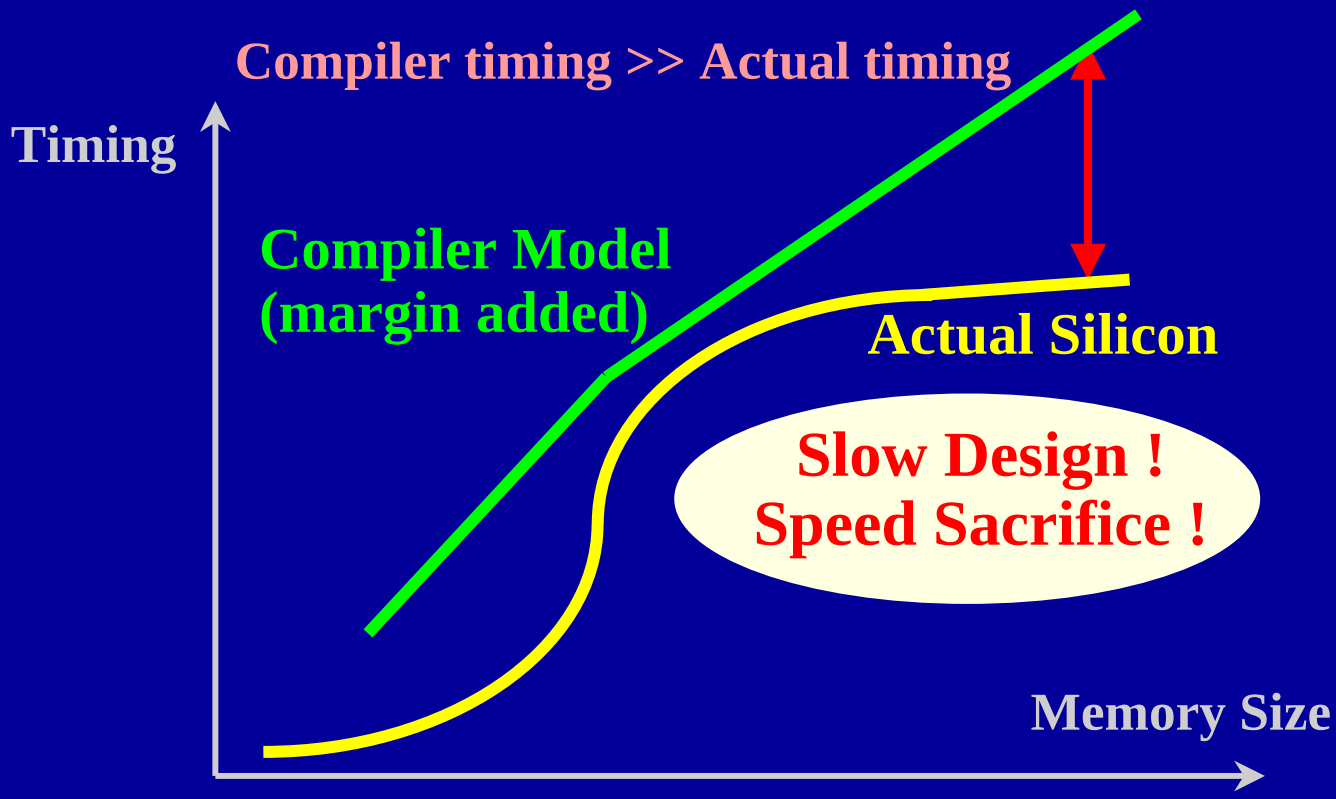
Compiler Model without Margin



MemChar™ can produce actual model !

Modeling Inaccuracy

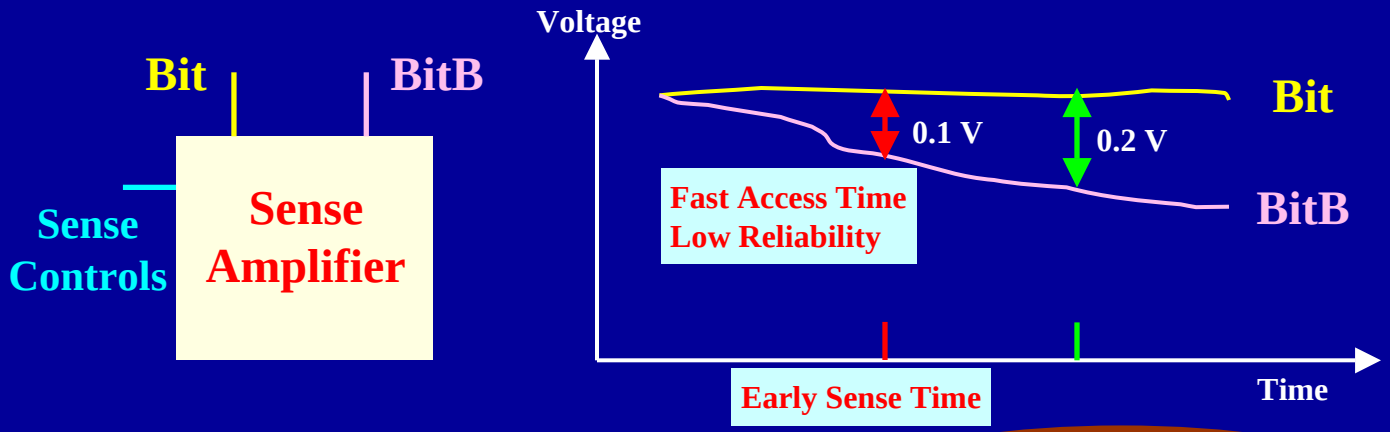
Compiler Model with Margin Added



MemChar™ can produce actual model !

Reliability Check

Sense-Amp Signal vs Internal Noise



- SpiceCut™ can locate
  - Bit and BitB signal
  - Sense control signal

Any change on power supply, .temp, process corners will impact Bit, BitB and Sense Controls.

- SpiceCut™ can automate the simulation output and measurement for reliability check

Benchmarks on Read Margin

Voltage(*Bit - BitB)* vs Access Time

- Legend's tools automate the reliability checking

0.18um SRAM 8Kx24

Read Margin	Sense Time	Access Time	V(Bit-BitB)	
1000	7.477 ns	4.3212 ns	365.8 mv	Slow
0100	5.040 ns	1.8824 ns	95.9 mv	
1101	5.977 ns	2.8109 ns	200.6 mv	
0111	5.040 ns	1.8824 ns	95.9 mv	
1111	4.790 ns	1.6969 ns	68.3 mv	Danger

** Noise margin is 100 mv minimum normally , and 200 mv for the safer.*

Wrong Read Margin (RM) setting causes Poor Yield!

Characterization/Simulation for In-house Compiler Developers

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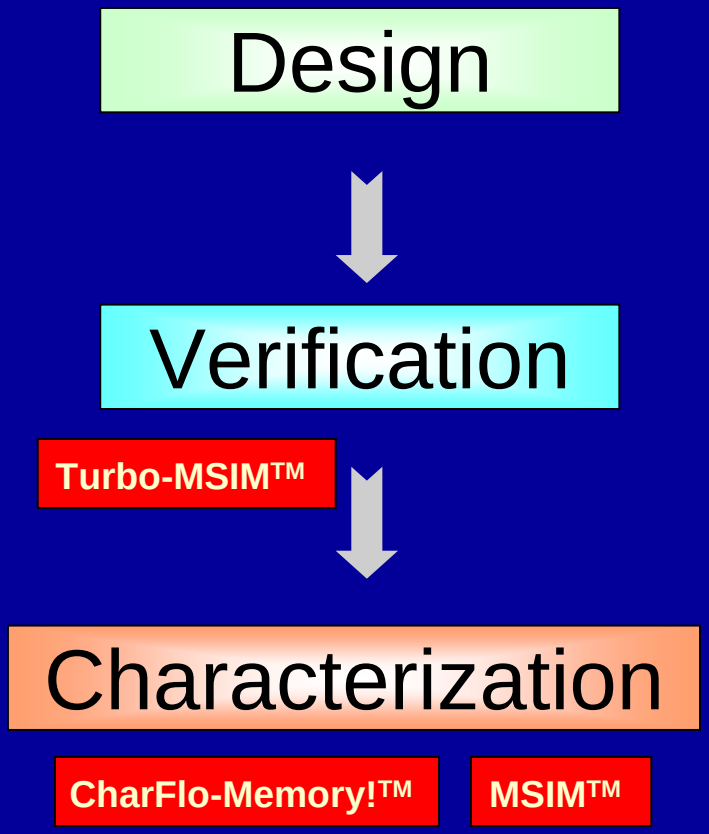
Memory Development Flow

Internal Memory Designs



Functional, Physical and Circuit Verification, IR Drop and EM Analysis

Critical-Path Identification

(Legend's SpiceCut-Memory)

- **Generate Timing and Power model**
  Access time, Setup and Hold time **etc.**
- **Build critical-path circuits**
- **Optimization for performance and reliability**

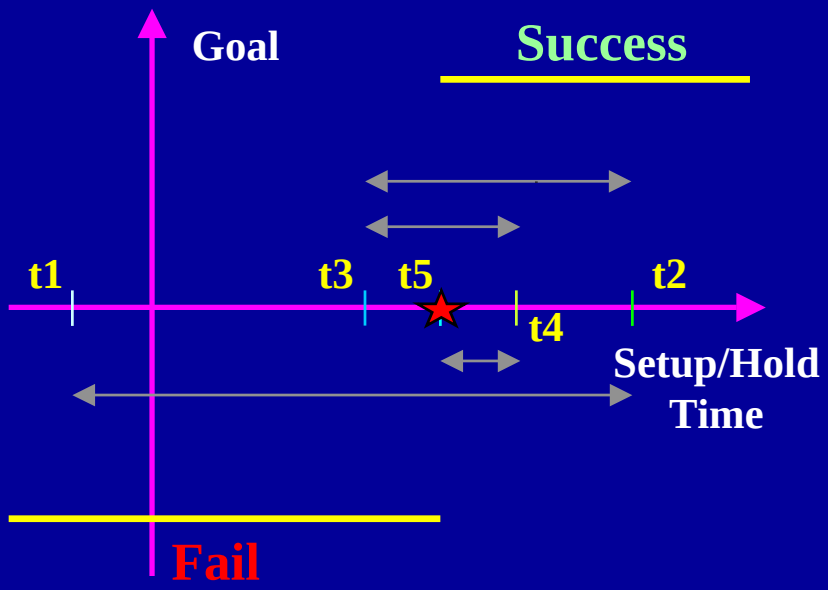
CharFlo-Memory!™
A Complete Solution

- ‘Bi-Section’ Mode
  - Setup/hold time from binary iterations
  - Glitch prevention and pulse-width checking
  - Accurate, optimized and automated
- ‘Path’ Mode
  - Setup/hold time from paths’ difference
  - Automated by latch pattern recognition

Bi-Section Mode

CharFlo-Memory!™

Bi-Section model in MemChar™ is based upon multi-criterion 'binary search' algorithm. The convergence is controlled by the 'BiSect Error'



t1 Start
t2 Start
t3 = (t1 + t2) / 2
t4 = (t2 + t3) / 2
t5 = (t3 + t4) / 2

Time	Goal	BiSect Error
t1	Fail	
t2	Success	Norm(t2-t1)
t3	Fail	Norm(t3-t2)
t4	Success	Norm(t4-t3)
t5	Success	Norm(t5-t4)

'Path' Mode

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Setup Time :

Data_Path - Clock_Path

where

Data_Path: Data-In -> Latch.OUT

Clock_Path: Clock -> Latch.CLK

Hold Time :

ClockB_Path - Data_Path

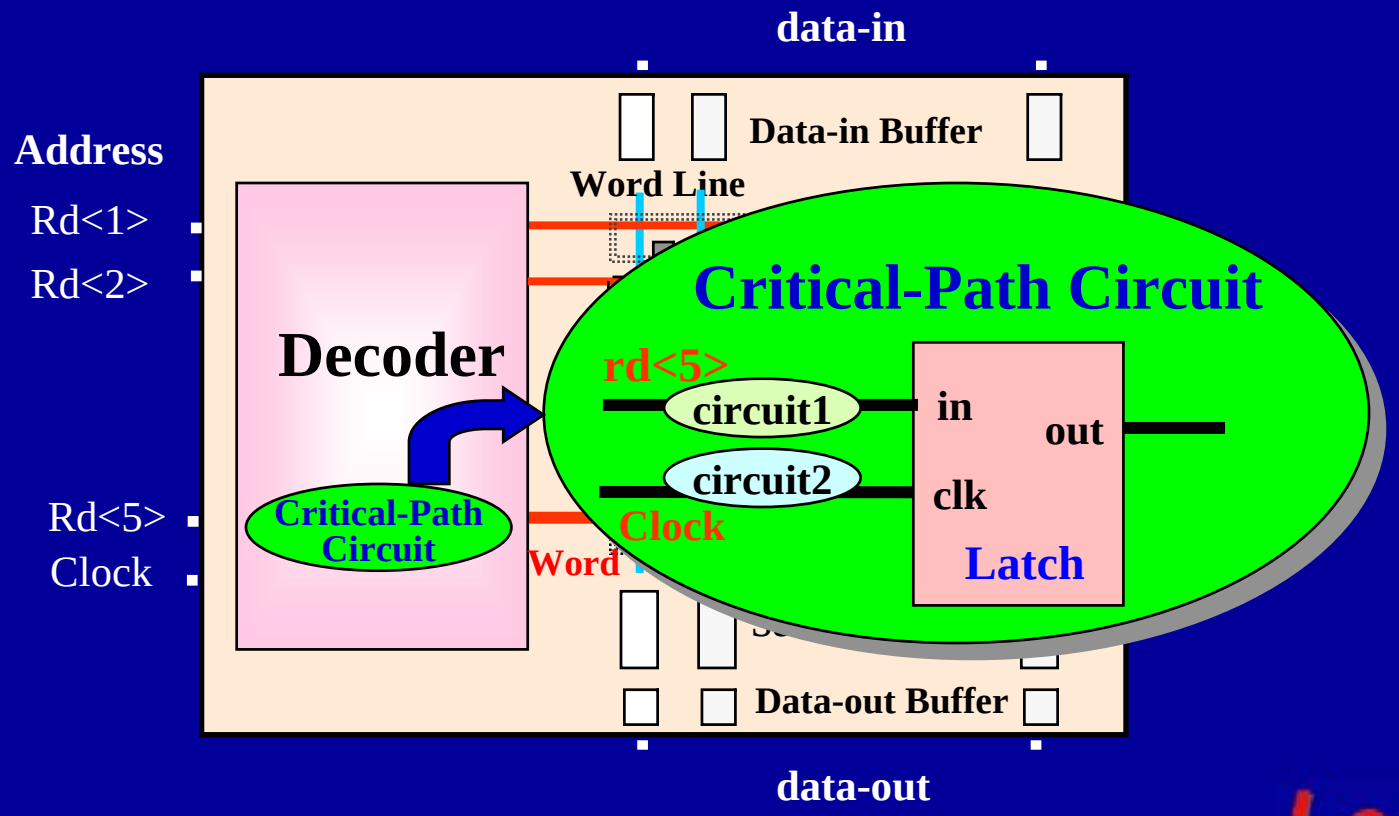
where

Data_Path: Data-In -> Latch.IN

ClockB_Path: Clock -> Latch.CLKB

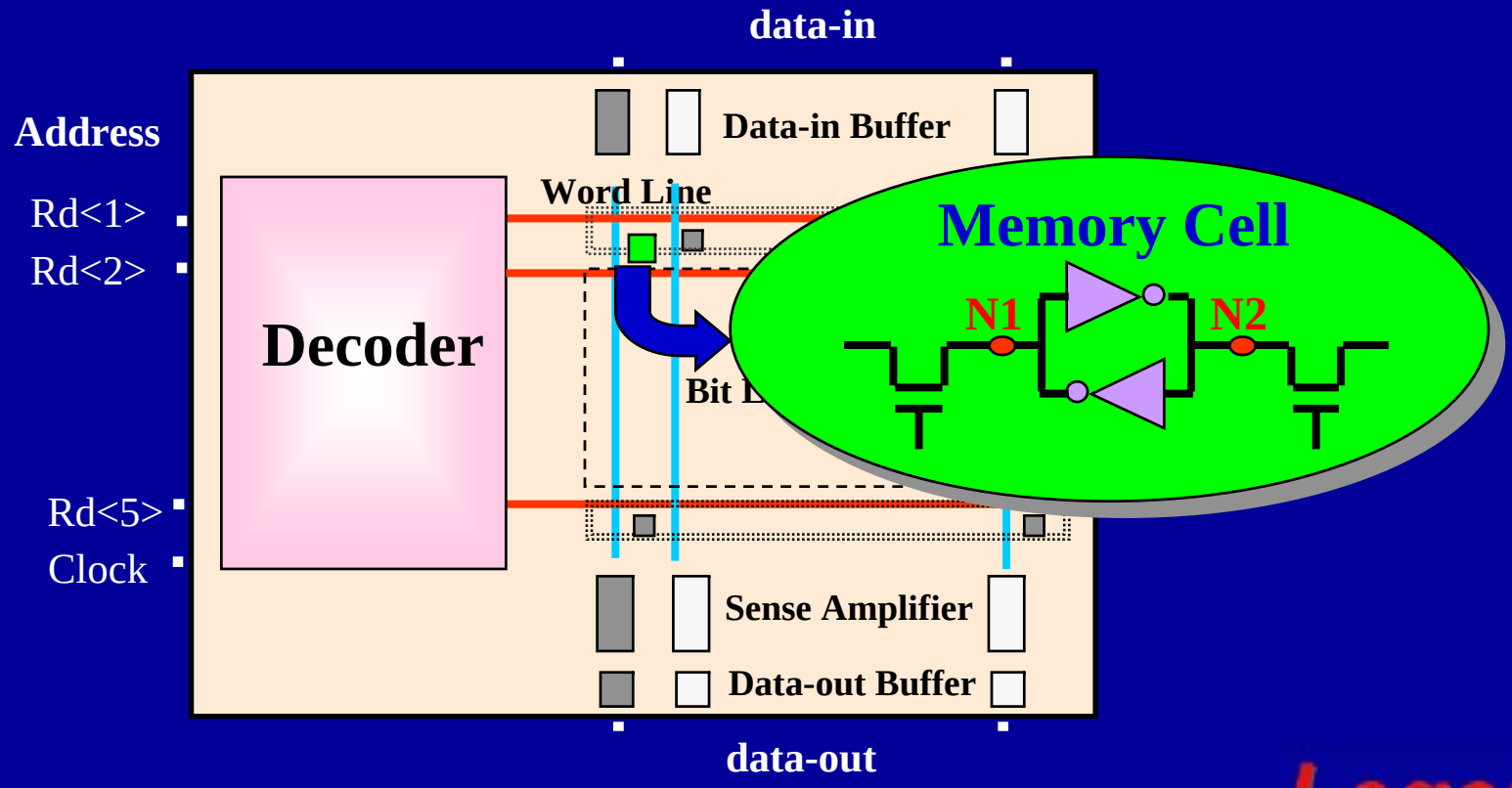
Address Setup / Hold Time

A ‘critical-path’ circuit can be automatically built for characterizing Address setup and hold time.



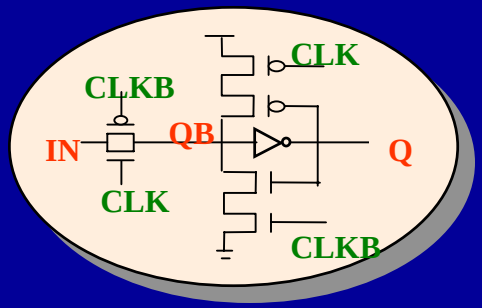
Measure Inside Cell

The internal node **N1** and **N2** of memory cells can be automatically located by Legend's tools.



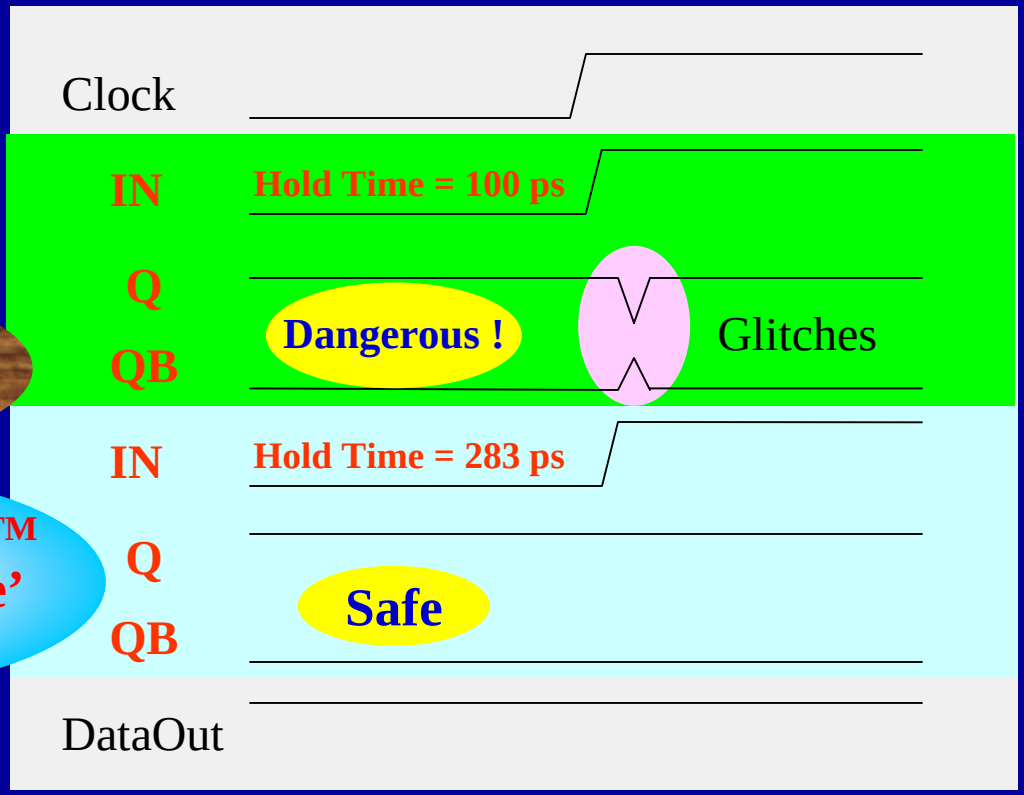
'Glitches' Prevention

Reliability Checking for Yield



Reliability Problem !

CharFlo-Memory™ locates 'glitch-free' setup/hold time



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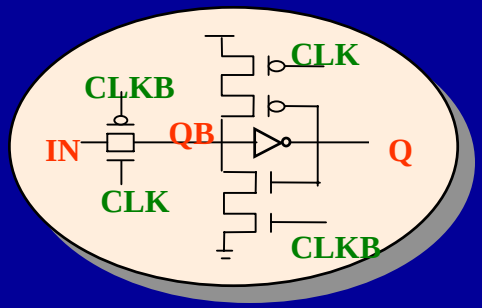
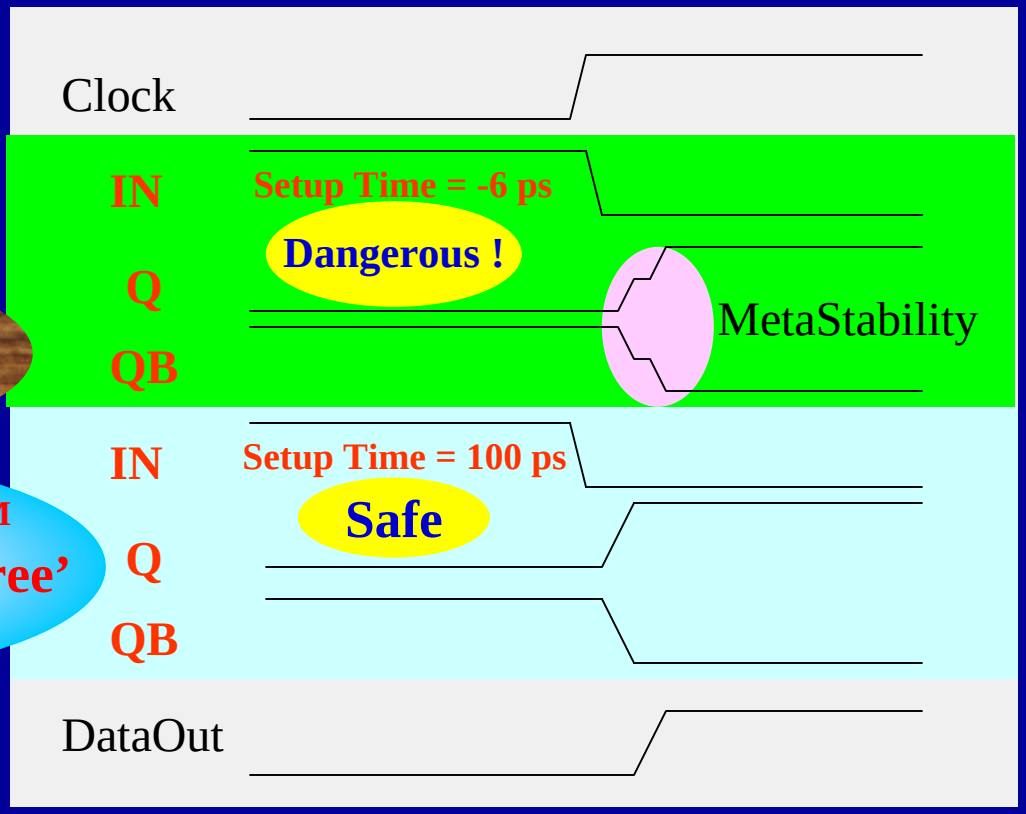
‘MetaStability’ Prevention

Reliability Checking for Yield



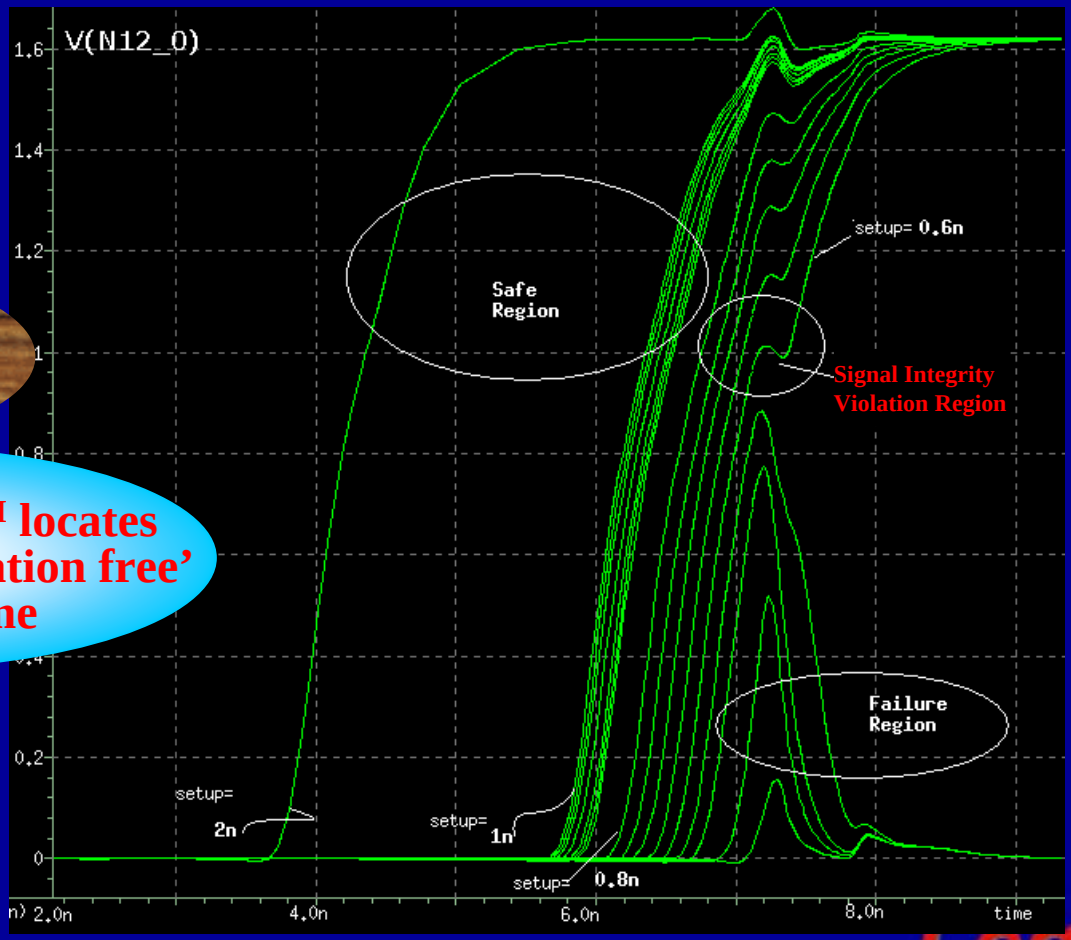
Reliability Problem !

CharFlo-Memory!™ locates ‘metastability free’ setup/hold time



‘Signal-Integrity’ Prevention

Reliability Checking for Yield



Reliability Problem !

CharFlo-Memory™ locates ‘Signal-Integrity violation free’ setup/hold time

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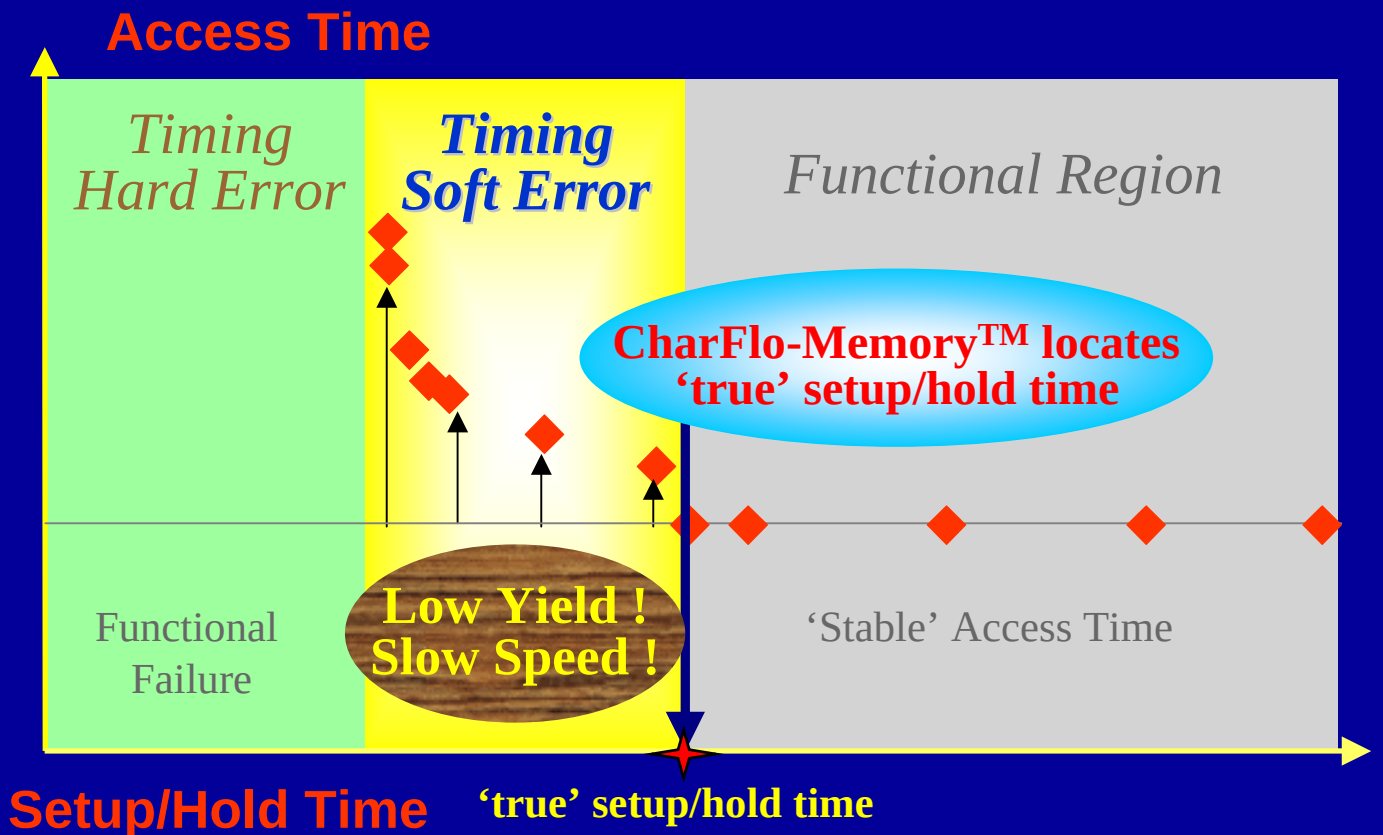
‘Timing Soft Error’ Prevention

Reliability Checking for Yield



SpiceCut Functions

CharFlo-Memory!™

- **Circuit characterization**

  Build ‘critical-path’ circuits for

  - Timing / Power simulations
  - Access / Setup / Hold Time / Minimum Clock

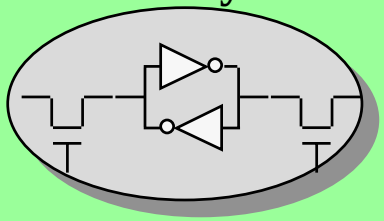
- **Circuit verification for**

  - Worst / best wordlines of decoders
  - Exhaustive address pattern simulation
  - Coupling analysis

- **Built-in RC reduction**

Recognize Memory Structure

Memory Cell

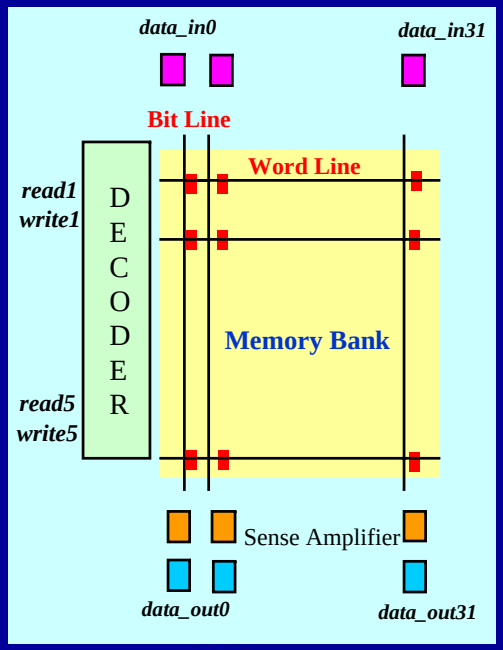


```
.subckt dual_cell 3 4 5 6 14 16
.alias word = 14
.alias bit = 5
.alias bitb = 4
.alias word2 = 16
.alias bit2 = 6
.alias bit2b = 3
M29   9    8    VDD   7    P  L=.40U
W=.60U
M30   VDD  9    8     7    P  L=.40U
W=.60U
M33   0    8    9     11   N  L=.40U  W=1.37U
M34   0    9    8     11   N  L=.40U  W=1.37U
M37   4    14   9     11   N  L=.40U  W=.85U
M38   5    14   8     11   N  L=.40U  W=.85U
M39   3    16   9     11   N  L=.40U  W=.85U
M40   6    16   8     11   N  L=.40U  W=.85U
.ENDS
```

- Pattern matching with core cell
- Locate all **memory banks**, **words** and **bits**

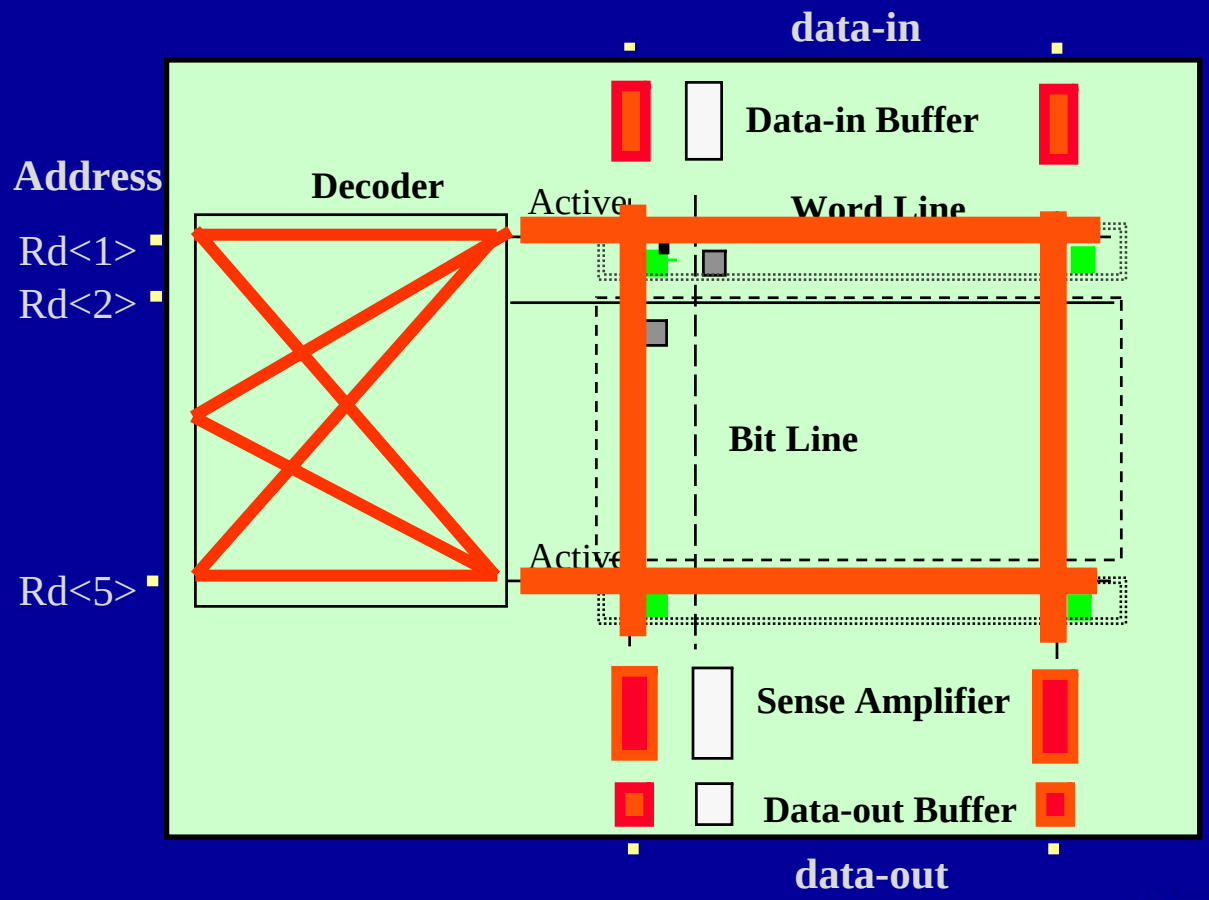
SpiceCut™

SpiceCut *Commands*

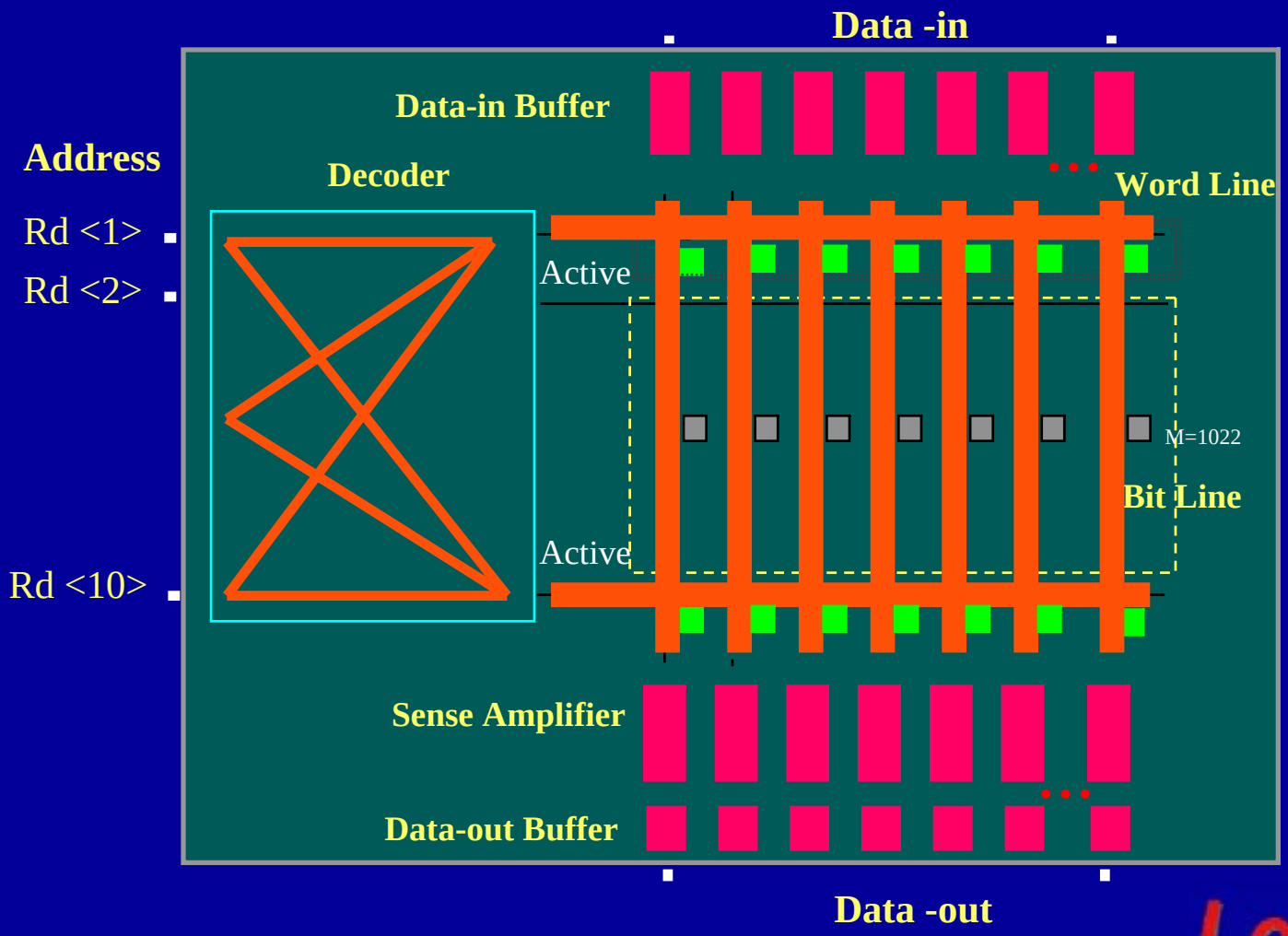


Build Critical-Path Circuit

‘Access Time’ Example



Critical-Path Circuit for Power



Circuit Simulation for Characterization and Verification

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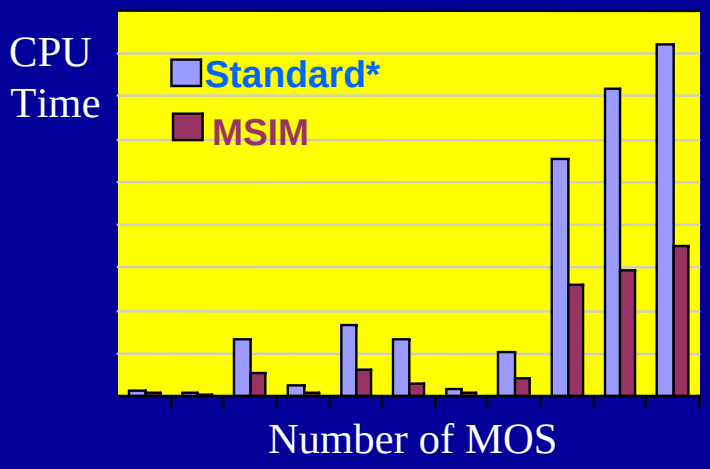
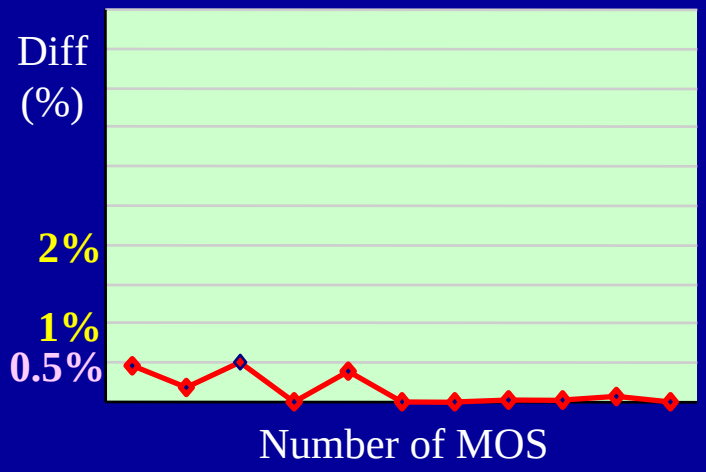
MSIM™

High Accuracy Spice Simulator

- More than twice speed of the Standard*
- Same accuracy (less than 1%) as the Standard*





** Standard means the most popular Spice simulator*

MSIM™
Benchmark Data

Full-Circuit 'Access Time' Simulation Results and Comparison

This 0.18um SRAM circuit has 21,087 MOS, 73,374 Rs and 44,639 Cs

Access Time	HSPICE Accurate Mode*	MSIM Accurate Mode		Standard** Simulator Default Mode		MSIM Default Mode	
	Time	Time	Difference	Time	Difference	Time	Difference
O[0] rise	1.4776ns	1.4769ns	-0.0474%	1.4541ns	-1.5904%	1.4849ns	0.4940%
O[24] rise	1.4832ns	1.4823ns	-0.0607%	1.4560ns	-1.8339%	1.4880ns	0.3236%
O[0] fall	1.5448ns	1.5441ns	-0.0453%	1.5219ns	-1.4824%	1.5552ns	0.6732%
O[24] fall	1.5446ns	1.5445ns	-0.0065%	1.5221ns	-1.4567%	1.5633ns	1.2107%

** **HSPICE Accurate Mode** is taken as 'GOLD' for comparison*

*** **Standard** means the most popular Spice circuit simulator*

Turbo-MSIM™

High Speed and High Capacity Simulator

- Full-chip simulations for SoC designs
- Memory and mixed-signal designs
- Timing and power analysis
- Hierarchical circuit simulation and verification
- Post-Layout circuit simulation and verification

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Turbo-MSIM™

Benchmark Data

Circuit Type: High-Speed SRAM (0.13um)

Type	MOS Count	Standard* Spice CPU Time	Turbo-MSIM CPU Time	Speed Up	Accuracy
Circuit 1	31,741	11,707 sec	37 sec	319 X	0.66 %
Circuit 2	57,079	21,483 sec	46 sec	467 X	1.50 %
Circuit 3	110,567	73,355 sec	78 sec	942 X	0.37 %
Circuit 4	1,619,735	N/A	756 sec	N/A	N/A
Circuit 5	3,198,065	N/A	1,636 sec	N/A	N/A
Circuit 6	6,395,298	N/A	5,725 sec	N/A	N/A

* ***Standard*** *means the most popular Spice circuit simulator*

The Conclusion

Legend's Characterization/Simulation Flow

- Production and silicon proven
- Automatically build critical-path circuits and structures from layout-extracted circuit with RC
- Feasible simulation time by any circuit simulator
- Access memory internals and reliability checking

  Check glitches, timing soft error, ReadMargin/Bit/BitB etc.
- RC reduction and ring-shape extraction for speed
- Foundry and IP vendors' support
- Excellent price-performance and automation